LOW NOISE AND LINEAR FET AMPLIFIERS FOR SATELLITE COMMUNICATIONS

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Abstract

FET Amplifiers with ambient noise figures as low as 4.8 dB at 12 GHz, 35 dB gain and intercept points as high as +28 dBm have been developed for use in communications satellites. Predicted mean time to failure is in excess of 10^6 hours.

Introduction

Two high reliability 12 GHz FET amplifiers have been developed for use in communications satellites. Over the operating temperature range, a low noise type showed a worst noise figure of 5.6 dB and a gain of 38 dB whilst a linear version had 35 dB gain with a third order intercept point of +23 dBm minimum. Complete results are available and will be presented on these units. Using improved FET's subsequently obtained from the supplier, a 0.4 dB improvement in noise figure and a 3 to 4 dB increase in intercept point have been achieved. Both amplifiers have good gain flatness, high gain stability with temperature and low group delay. Small size, light weight and low power consumption from a single +15V dc supply rail are important features.

Device Selection and Characterization

The transistor selected for the FET amplifiers was the Nippon NE24406, a one micron gate-length device in a hermetic ceramic package. Stringent qualification testing of flight devices included power burn-in for 336 hours at 100°C ambient with dc and rf parameters monitored; $\pm 5\% \Delta I_{DSS}$ was permitted and ± 0.1 dB Δ MAG. Short and medium term stability were evaluated by mounting five sample devices from each wafer into an amplifier. A maximum gain drift of 0.1 dB per decade of time was permitted over a 1,000 hour test period (Fig. 1). Other qualification tests included 100% Group A tests and Group B testing on wafer sample devices, with a reliability assessment based on accelerated life testing at 295°C. All flight devices were checked for short term ($t < 100$ min.) drift characteristics (dc and rf) following the power burn-in.

For the computer-aided design techniques used it was essential to perform accurate S-parameter measurements. The transistor test mount was characterized on an Automatic Network Analyzer before mounting transistors, and an equivalent circuit derived; this was used in the correction of transistor S-parameters to a convenient design reference plane.

Optimum source impedance for low noise performance was determined empirically and found to be close to a conjugate match to the transistor. The optimum load impedance for intermodulation products was also determined empirically by tuning for maximum saturated power output.

Amplifier Design

A single-ended modular design appraoch which provides 'drop-in' amplifier integration of the pre-tuned modules was used. Advantages over balanced designs include lower cost (significant for flight qualified devices), higher reliability due to a lower component count, and lower power consumption. Each of the two amplifier types contains three two-stage amplifier modules (six FETs) with isolator modules between them and at both amplifier ports. A P.I.N. attenuator module located either before or after the second amplifier module (depending on the amplifier type) provides amplifier gain-temperature compensation with very small gain slope variation. Its position was chosen to have a minimal effect on noise figure of the low noise amplifier (Fig. 2) and on intermodulation products in the linear amplifier.

The three two-stage amplifier module types were designed using typical measured S-parameter data, with the aid of an RCA network analysis-optimization computer program COSMIC-K.

The MIC isolator modules are three-port circulators printed on Yttrium Garnet substrates, with a 50 ohm chip resistor terminating the third port. Isolation is enhanced by suppressing radiation from the circulator disc. A minimum isolation of 26 dB with less than 0.3 dB insertion loss is achieved.

Each P.I.N. attenuator module comprises two series mounted beam lead diodes (a 'fail safe' configuration since P.I.N. diodes normally fail short circuit) spaced approximately one-quarter wavelength apart for low VSWR. The drive circuit consists of a thermistor controlled current source whose resistor elements are computer optimized to a achieve the best temperature compensation curve fit.

The common-source FET mounting configuration used requires both positive and negative voltage bias rails for each transistor. A switching regulator provides greater than 75% power conversion efficiency from the available +15V supply voltage to a +5.7V drain and P.I.N. attenuator drive supply and a -5.0V gate supply. A slow start-up circuit is employed to prevent voltage overshoots. High regulation is obtained by using high stability components and high feedback loop gain. Filter networks give low ripple on the bias rails and prevent current overshoots.

Amplifier and P.I.N. attenuator modules are constructed of 0.025 inch thick 99.5% Alumina substrates, soldered to nickel plated Kovar carriers, and the isolator

modules are constructed with 0.025 inch garnet substrates soldered to a nickel plated Nickel/Iron alloy carrier. The thermal expansion coefficient of substrates and carriers are closely matched to reduce temperature cycling stresses. Stress-relieved bonds are used to interconnect modules. The overall amplifier size is approximately three and one-half ($3\frac{1}{2}$) inches square by one inch deep (Fig. 6).

Amplifier Reliability

All components and materials used in the amplifiers are subjected to the usual screening requirements for use in high reliability applications.

Accelerated life testing by the device manufacturer has shown FETs to be inherently highly reliable devices.[1] For the complete amplifier, including power converter, a failure rate of 876 FITS (failures in 10^9 hours) is predicted; this assumes a failure rate of 64 FITS for each transistor (maximum channel temperature 82°C). Worst case analysis for a seven year operational life gives a worst case gain stability of +.61 dB, -1.09 dB. The change in noise figure and linearity performance is not significant.

It is estimated that the ionizing radiation dose absorbed by the devices will be limited to 10^5 rads by the spacecraft structure and amplifier and receiver enclosures, and that particle fluence will not exceed $2 \times 10^{13}/cm^2$. These figures are well below the thresholds at which damage to FETs has been recorded.[2,3]

Measured Performance (Table 1)

A complete set of results were recorded using some early FET devices. These are presented below. Using better FETs subsequently obtained from the supplier, a 0.4 dB noise figure improvement and a 3 to 4 dB higher intercept point were achieved.

The significant electrical parameters were recorded over several temperature cycles with extremes ±10°C in excess of the 0-50°C design temperature range. The high gain slope stability with temperature is a result of employing constant FET bias and a well matched P.I.N. diode attenuator for temperature compensation (Fig. 4).

The worst case intercept point of the linear amplifier was +23.2 dBm (Fig. 5). No variation was observed with changing carrier separation (0.5 to 50 MHz Δf was tested) indicating effective decoupling of the converter supply from the rf circuitry.

A worst case noise figure of 5.6 dB was measured at 50°C for the low noise amplifier (Fig. 3). This performance was achieved by selection of the front-end FETs which have a 3.9 dB noise figure at 25°C and by minimizing the loss of the input isolator.

The group delay variation was very small. At the temperature extremes it is 0.4 nsec and 0.5 nsec over the 500 MHz band for the low noise and linear amplifiers respectively.

Amplifier power consumptions varied less than 5% over the operating temperature range. This reflects the low current requirement of the P.I.N. attenuator, the use of constant FET bias, and the relatively constant converter efficiency over the temperature range.

Conclusion

It is felt that these amplifiers represent the state of the art for high reliability amplifiers in this frequency range. The probability of survival for such amplifiers over communications satellite lifetimes is at least as high as alternative types of amplifiers that are currently available, and it is likely that they will find increasing application in high reliability systems

Acknowledgements

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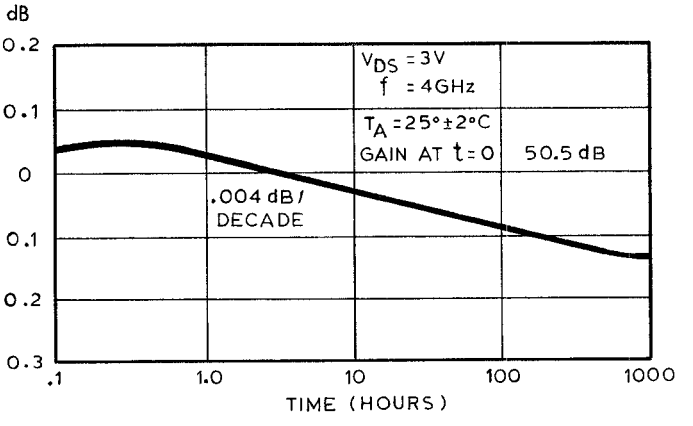

Fig. 1: Gain Drift for 5-stage Amplifier

TABLE 1: SPECIFICATION AND PERFORMANCE SUMMARY

Parameter	Specification		Measured Performance (Worst Case over Spec. Temperature Range)	
Operating Frequency Range 11.7-12.2 GHz (unless otherwise stated)	Parameter Specification	Applicable Temperature Range (°C)	Low Noise Amplifier	Linear Amplifier
Midband Gain	35 dB + 2, -0 dB	25	38.65 dB	35.75 dB
Gain Variation over Frequency Band	1.0 dB Peak-to-Peak maximum	0-50	0.40 dB	0.50 dB
Gain Stability	1.25 dB Peak-to-Peak maximum	5-45	0.80 dB	0.50 dB
Gain Slope	.004 dB/MHz maximum	0-50	0.003 dB/MHz	0.0032 dB/MHz
Noise Figure	7 dB maximum (Low Noise) 10 dB maximum (Linear)	0-50	5.6 dB	9.5 dB
Port VSWR	1.25:1 maximum	0-50	1.11:1 Input Port 1.10:1 Output Port	1.20:1 Both Ports
Group Delay Variation	0.5 ns maximum	0-50	0.4 ns	0.5 ns
Linearity	3rd order intercept point +17 dBm minimum (Low Noise) +23 dBm maximum (Linear)	0-50	+20.3 dBm	+23.2 dBm
Spurious Outputs	-75 dBm maximum	0-50	None detectable	None detectable
Power Consumption	1.5W maximum	0-50	1.09W	1.27W
Voltage Variation	15V ± 5%	0-50	No measureable effect on gain frequency response, noise figure, linearity.	
Weight	0.75 lb maximum	—	0.84 lb	0.84 lb

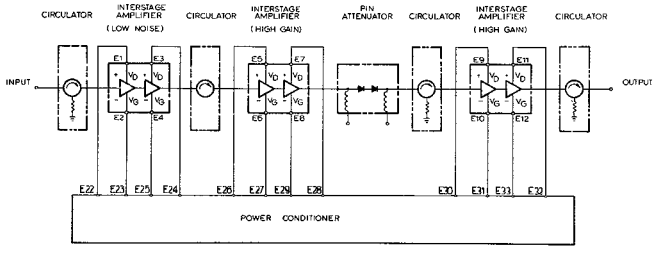

Fig. 2: Low Noise Amplifier Schematic

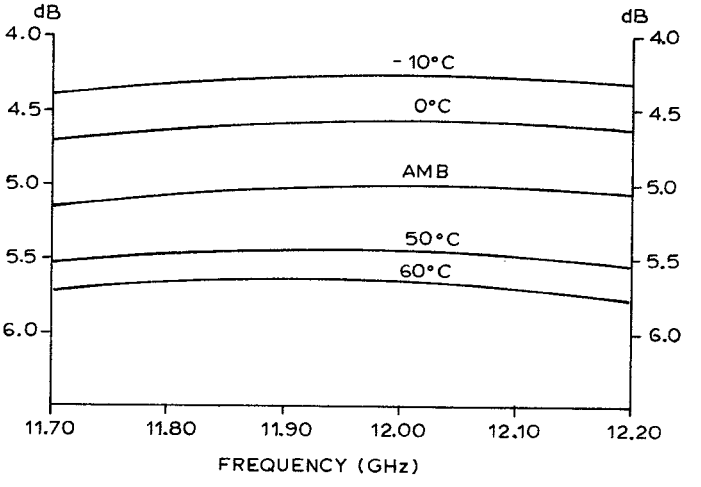

Fig. 3: Low Noise Amplifier Noise Figure

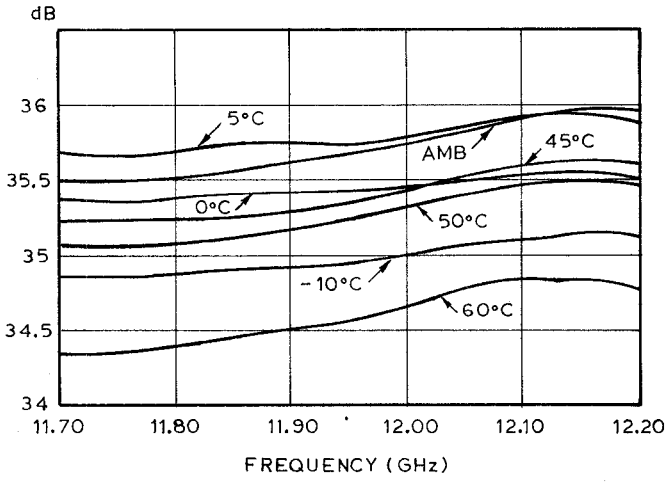

Fig. 4: Linear Amplifier Gain with P.I.N. Diode Compensation

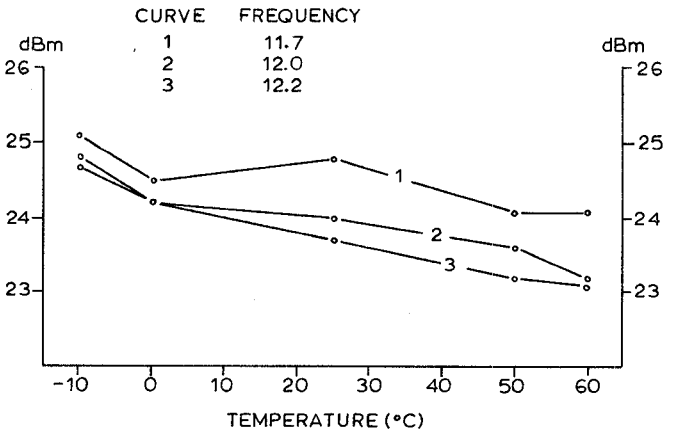

Fig. 5: Linear Amplifiers Intercept Point

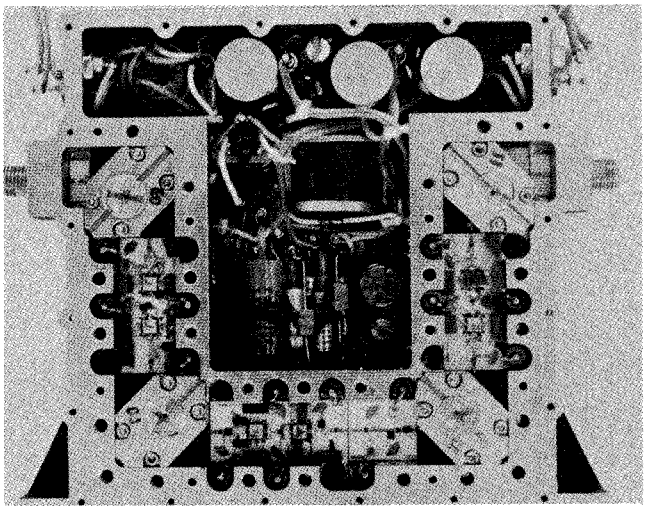

Fig. 6: Photograph of the Linear Amplifier with Top Cover Removed